**ECE3410 Lab 5**

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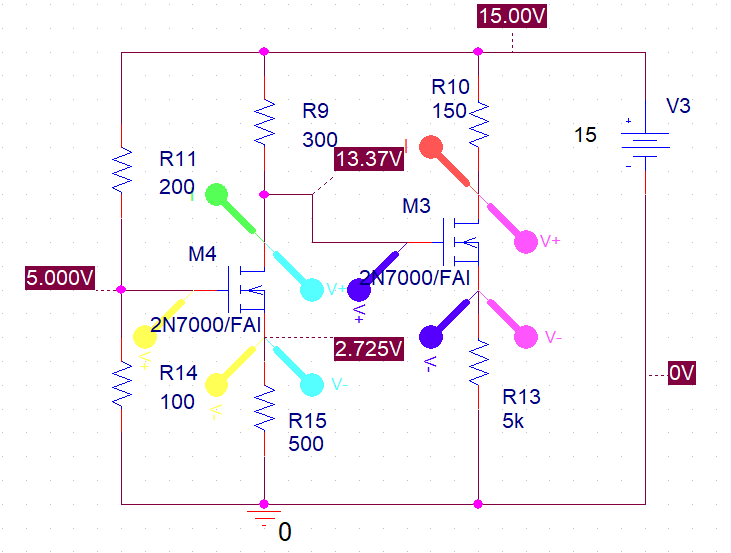
**Objective**

The objective of this lab was to study FET cascade amplifier characteristics and circuit design. We looked at the biasing points, AC and DC characteristics, and the gain across each transistor.

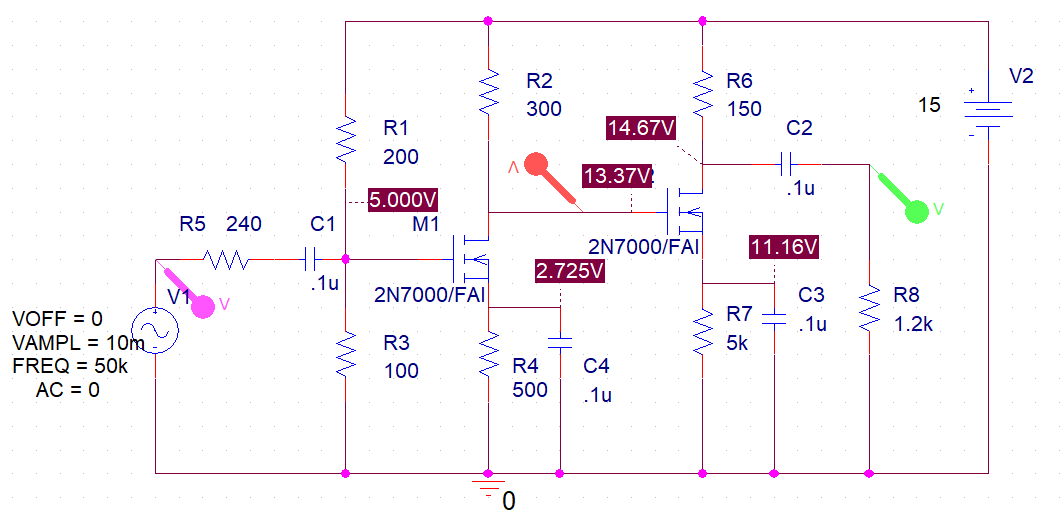
**Description**

In PSpice I used 2 2N7000 Fairchild Transistors with the gate of the second connected to the drain of the first. The output load resistor was coupled to the drain of the second transistor with a .1uF capacitor. A 15V DC source connected to the drain resistors of each transistor and to the gate of the first through a 2 resistor voltage divider. The AC input was coupled to the first transistor’s gate via another .1uF capacitor. The Sources of both transistors connected to resistors and then to ground.

**Circuit Diagrams**

**DC Circuit**

**AC Circuit**

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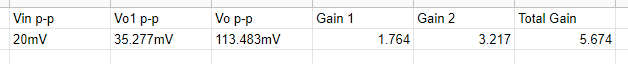
**Process**

* Simulate Circuit in PSpice
* Find the DC Characteristic values, and the voltages at gate 2 and vo.
* Calculate the gain at gate 2, and the overall gain.
* Construct the circuit on breadboard.
* Find the DC values for the real circuit using the multimeter.
* Find the output voltages using the Oscilloscope.
* Compute the actual gain at gate 2 and vo and calculate the real gain.
* Compare with simulation.

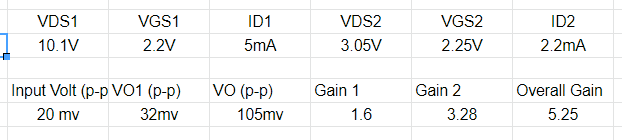
**Table of Measurements**

**PSpice Data**

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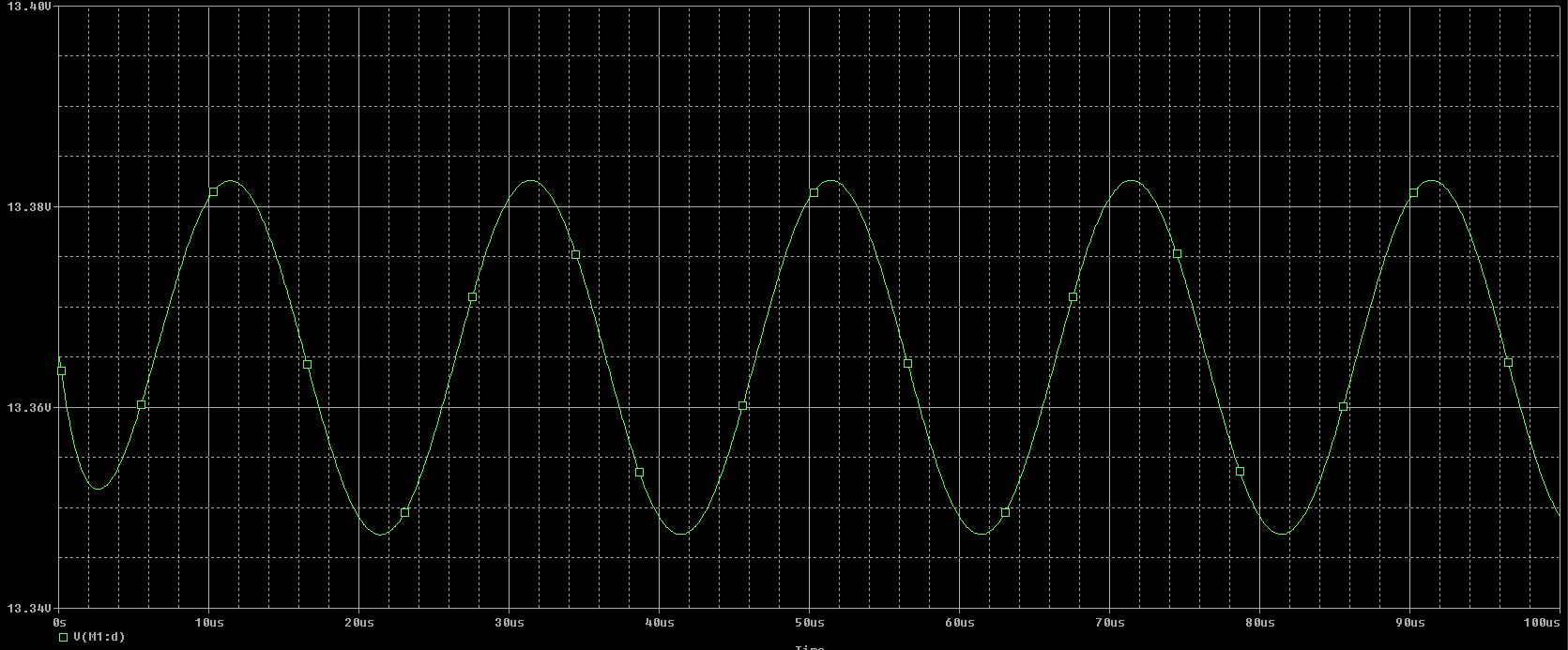
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**Breadboard Data**

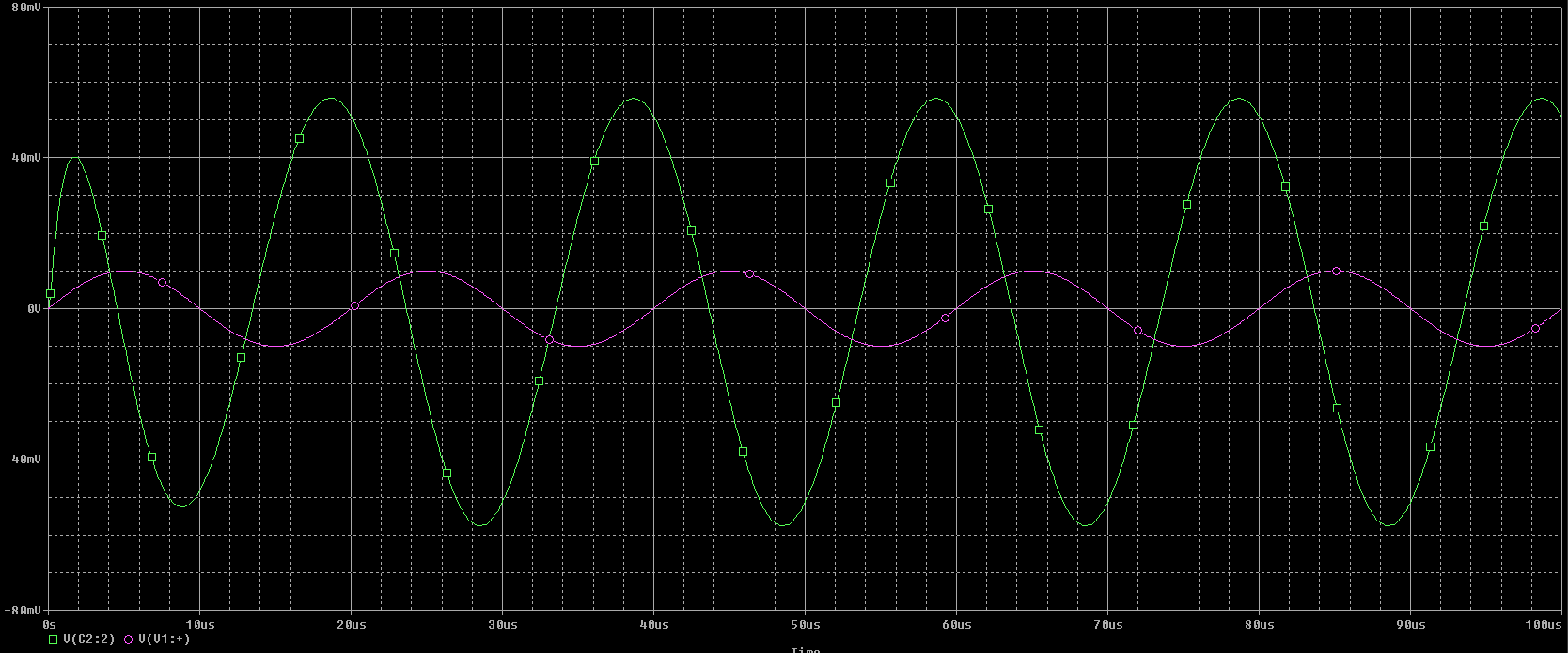
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**Characteristics and Plots**

**PSpice Vo1**

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**PSpice Vo and Vs**

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**Breadboard Result**

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**Explanation of Plots and Results**

The first simulation plot shows the voltage at vo1, the 2nd gate, being offset by 13.37V, the DC voltage at the node. However, Vp-p for the small signal is 35.277mV giving a small gain of 1.764. The second plot shows the input voltage in magenta, and vo in green. The total gain is 5.674. The Oscilloscope shows similar results for the breadboard circuit. The real circuit values are quite close to the simulation values. The actual output is a few mV lower than the simulation making the total gain lower, and VDS1 and 2 are higher in the simulation as well. These differences are likely not significant for this experiment, and are probably due to variance in the real components from the ideal simulations.

**Summary**

In this lab, we looked at the FET cascade amplifier circuit and found the gain to be much higher than over a single transistor. The total gain is equal to gain1 times gain 2. The Output is out of phase with the input due to the capacitor couplings and delay in FET switching, but otherwise the results were fairly similar in the simulation and circuit.